What is claimed is:

1. An amplifier circuit comprising;

a first amplifier, outputting internal signals in response to input signals and changing a common mode voltage level defined by the internal signals in response to control signals; and

a second amplifier, comparing voltage levels of the internal signals, outputting an output signal in accordance with a comparison result, and changing a duty cycle of the output signal in accordance with changes in the common mode voltage level of the internal signals.

2. The amplifier circuit of claim 1, wherein the first amplifier changes a voltage of one of the internal signals in response to the control signals, thereby changing the common mode voltage level of the internal signals.

3. The amplifier circuit of claim 1, wherein the first amplifier further comprises:

a differential amplifier, comprising a load circuit comparing the voltage levels of the input signals, and outputting the internal signals in accordance with a comparison result; and

a common mode control circuit connected in parallel with the load circuit and changing the common mode voltage level of the internal signals in response to the control signals.

4. The amplifier circuit of 3, wherein the load circuit further comprises a first load connected between a first node and a second node and a second load connected between the first node and a third node, and wherein the common mode control circuit further comprises:

a first common mode change circuit connected in parallel with the first load and changing a resistance between the first node and the second node in response to first control signals among the control signals; and

a second common mode change circuit connected in parallel with the second load and changing a resistance between the second node and the third node in response to second control signals among the control signals.

5. The amplifier circuit of 4, wherein the first common mode change circuit further comprises:

a plurality of first NMOS transistors having drains connected to the first load, sources connected to the second node, and gates connected respectively to the first control signals are input; and,

wherein the second common mode change circuit further comprises a plurality of second NMOS transistors having drains connected to the first node, sources connected to the third node, and gates connected respectively to the second control signals.

6. The amplifier circuit of 5, wherein the internal signals include a first internal signal and a second internal signal complementary to the first internal signal, and

wherein, upon enabling one or more of the first control signals, the one or more of the plurality of first NMOS transistors are turned on, and wherein, upon enabling one or more of the second control signals, one or more of the plurality of second NMOS transistors are turned on, such that

upon increasing the number of NMOS transistors in the plurality of first NMOS transistors turned off, a voltage level of the second internal signal correspondingly decreases, and upon increasing the number of NMOS transistors in the plurality of second NMOS transistors turned off , a voltage level of the first internal signal correspondingly decreases.

7. The amplifier circuit of claim 6, wherein as the voltage level of the second internal signal decreases, a duty cycle of the output signal correspondingly decreases, and as the voltage level of the first internal signal decreases, the duty cycle of the output signal correspondingly increases.

8. A replica delay circuit adapted for use in an internal clock generator, the replica delay circuit receiving an external clock signal and outputting an internal clock, and comprising:

a circuit adapted to synchronize a phase difference between the external clock signal and a reference clock signal, wherein the internal clock signal is derived in relation to the phases difference;

a first replica delay unit, delaying the internal clock signal for a predetermined period of time and generating first delay clock signals; and

a second replica delay unit, generating the reference clock signal in response to the first delay clock signals and changing a duty cycle of the reference clock signal in response to selected control signals.

9. The replica delay circuit of claim 8, where the second replica delay unit further comprises:

a first amplifier generating second delay clock signals in response to the first delay clock signals and changing a common mode voltage level for the second delay clock signals in response to the selected control signals; and

a second amplifier, comparing voltage levels for the second delay clock signals, outputting the reference clock signal in accordance with a comparison result, and changing the duty cycle of the reference clock signal in accordance with changes in the common mode voltage level of the second delay clock signals.

10. The replica delay circuit of claim 9, wherein the first amplifier further comprises:

a differential amplifier, comprising a load circuit, and comparing voltage levels for the first delay clock signals, and generating the second delay clock signals in accordance with a comparison result; and

a common mode control circuit, connected in parallel with the load circuit and changing the common mode voltage level of the second delay clock signals in response to selected control signals.

11. The replica delay circuit of claim 10, wherein the load circuit further comprises a first load connected between a first node and a second node and a second load connected between the first node and a third node, and

wherein the common mode control circuit further comprises:

a first common mode change circuit, connected in parallel with the first load and changing a resistance between the first node and the second node in response to first control signals among the selected control signals; and

a second common mode change circuit, connected in parallel with the second load and changing a resistance between the second node and the third node in response to second control signals among the selected control signals.

12. The replica delay circuit of claim 11, wherein the first common mode change circuit further comprises:

a plurality of first NMOS transistors having drains connected to the first load, sources connected to the second node, and gates respectively receiving selected first control signals, and;

wherein the second common mode change circuit comprises a plurality of second NMOS transistors have drains connected to the first node, sources connected to the third node, and gates respectively receiving selected second control signals.

13. The replica delay circuit of claim 12, wherein the second delay clock signals include a first clock signal and a second clock signal complementary to the first clock signal, such that

upon enabling selected first control signals, at least one of the plurality of first NMOS transistors is turned on, and upon enabling selected second control signals, at least one of the plurality of second NMOS transistors is turned on, such that

as the number of transistors turned off in the plurality of first NMOS transistors increases, a voltage level of the second clock signal decreases, and as the number of transistors turned off in the plurality of second NMOS transistors increases, a voltage level of the first clock signal decreases.

14. The replica delay circuit of claim 13, wherein as the voltage level of the second clock signal decreases, a duty cycle of the reference clock signal decreases. and as the voltage level of the first clock signal decreases, the duty cycle of the reference clock signal increases.

15. An internal clock generator receiving an external clock signal and generating an internal clock signal in relation to a phase difference determined in relation to a phase/delay lock comparison between the external clock signal and an internally generated reference clock signal, the internal clock generator comprising:

a variable delay circuit delaying the external clock signal for a first predetermined period of time and generating a delayed external clock signal;

a buffer circuit amplifying the delayed external clock signal and generating the internal clock signal;

a replica delay circuit delaying the internal clock signal for a second predetermined period of time, generating the reference clock signal, and changing a duty cycle of the reference clock signal in response to control signals;

a control signal generator generating the control signals in accordance with a phase offset between the internal clock signal and the external clock signal; and

a phase detector detecting a phase difference between the external clock signal and the reference clock signal and controlling the first predetermined amount of time of the variable delay circuit in accordance with a detection result.

16. The internal clock generator of claim 15, wherein the replica delay circuit further comprises:

a first replica delay unit delaying the internal clock signal for a third predetermined period of time and generating first delay clock signals; and

a second replica delay unit generating the reference clock signal in response to the first delay clock signals and changing a duty cycle of the reference clock signal in response to control signals.

17. The internal clock generator of claim 16, wherein the second replica delay unit further comprises:

a first amplifier generating second delay clock signals in response to the first delay clock signals and changing a common mode voltage level for the second delay clock signals in response to the control signals; and

a second amplifier comparing voltage levels of the second delay clock signals, generating the reference clock signal in accordance with a comparison result, and changing the duty cycle of the reference clock signal as the common mode voltage level of the second delay clock signals is changed.

18. The internal clock generator of claim 17, wherein the first amplifier further comprises:

a differential amplifier, comprising a load circuit, comparing voltage levels of the first delay clock signals, and generating the second delay clock signals in accordance with a comparison result; and

a common mode control circuit, connected in parallel with the load circuit and changing the common mode voltage level of the second delay clock signals in response to the control signals.

19. The internal clock generator of claim 18, wherein the load circuit comprises a first load connected between a first node and a second node and a second load connected between the first node and a third node, and the common mode control circuit further comprises:

a first common mode change circuit, connected in parallel with the first load and changing a resistance between the first node and the second node in response to first control signals among the control signals; and

a second common mode change circuit, connected in parallel with the second load and changing a resistance between the first node and the third node in response to second control signals among the control signals.

20. The internal clock generator of claim 19, wherein the first common mode change circuit comprises a plurality of first NMOS transistors having drains connected to the first node, sources connected to the second node, and gates respectively receiving selected first control signals, and

wherein the second common mode change circuit comprises a plurality of second NMOS transistors have drains connected to the first node, sources connected to the third node, and gates respectively receiving selected second control signals.

21. The internal clock generator of claim 20, wherein the second delay clock signals comprises a first clock signal and a second clock signal complementary to the first clock signal, wherein as at least one of the first control signals is enabled, at least one of the plurality of first NMOS transistors is turned on, and as at least one of the second control signals is enabled, at least one of the plurality of second NMOS transistors is turned on, such that as the number of transistors turned on in the plurality of first NMOS transistors increases, a voltage level of the second clock signal decreases, and as the number transistors turned off in the plurality of the second NMOS transistors increases, a voltage level of the first clock signal decreases.

22. The internal clock generator of claim 21, wherein as the voltage level of the second clock signal decreases, a duty cycle of the reference clock signal correspondingly decreases, and as the voltage level of the first clock signal decreases, the duty cycle of the reference clock signal correspondingly increases.